

# RJK03P7DPA

MOS1 30 V, 15 A, 9.4 mΩ max.

MOS2 30 V, 30 A, 5.3 mΩ max.

Built in SBD Dual N-channel Power MOS FET

High Speed Power Switching

R07DS0906EJ0110

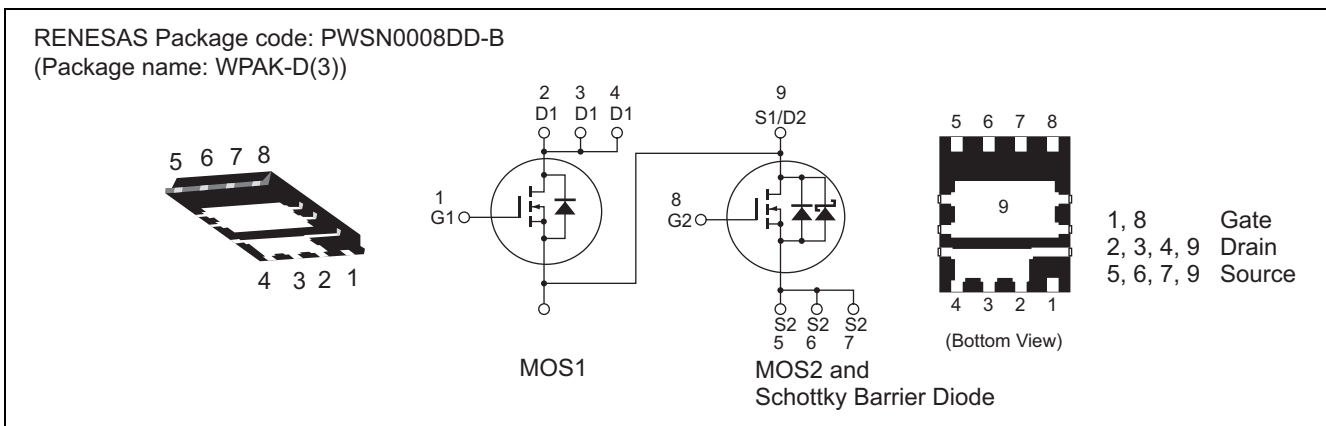
Rev.1.10

Nov 01, 2012

## Features

- Low on-resistance
- Capable of 4.5 V gate drive
- High density mounting
- Pb-free
- Halogen-free

## Outline



## Absolute Maximum Ratings

(Ta = 25°C)

Item	Symbol	Ratings		Unit
		MOS1	MOS2	
Drain to source voltage	V <sub>DSS</sub>	30	30	V
Gate to source voltage	V <sub>GSS</sub>	±20	±20	V
Drain current	I <sub>D</sub>	15	30	A
Drain peak current	I <sub>D(pulse)</sub> <sup>Note1</sup>	60	120	A
Reverse drain current	I <sub>DR</sub>	15	30	A
Avalanche current	I <sub>AP</sub> <sup>Note 2</sup>	8.5	12	A
Avalanche energy	E <sub>AS</sub> <sup>Note 2</sup>	7.23	14.4	mJ
Channel dissipation	P <sub>ch</sub> <sup>Note3</sup>	10	20	W
Channel temperature	T <sub>ch</sub>	150	150	°C
Storage temperature	T <sub>stg</sub>	-55 to +150	-55 to +150	°C

Notes: 1. PW ≤ 10 μs, duty cycle ≤ 1%

2. Value at T<sub>ch</sub> = 25°C, R<sub>g</sub> ≥ 50 Ω

3. T<sub>c</sub>=25°C

## Electrical Characteristics

## • MOS1

(Ta = 25°C)

Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	30	—	—	V	$I_D = 10 \text{ mA}, V_{GS} = 0$
Gate to source leak current	$I_{GSS}$	—	—	$\pm 0.5$	$\mu\text{A}$	$V_{GS} = \pm 20 \text{ V}, V_{DS} = 0$
Zero gate voltage drain current	$I_{DSS}$	—	—	1	$\mu\text{A}$	$V_{DS} = 24 \text{ V}, V_{GS} = 0$
Gate to source cutoff voltage	$V_{GS(off)}$	1.2	—	2.5	V	$V_{DS} = 10 \text{ V}, I_D = 1 \text{ mA}$
Static drain to source on state resistance	$R_{DS(on)}$	—	7.8	9.4	$\text{m}\Omega$	$I_D = 7.5 \text{ A}, V_{GS} = 10 \text{ V}$ <sup>Note4</sup>
	$R_{DS(on)}$	—	9.7	12.6	$\text{m}\Omega$	$I_D = 7.5 \text{ A}, V_{GS} = 4.5 \text{ V}$ <sup>Note4</sup>
Forward transfer admittance	$ y_{fs} $	—	36	—	S	$I_D = 7.5 \text{ A}, V_{DS} = 5 \text{ V}$ <sup>Note4</sup>
Input capacitance	$C_{iss}$	—	850	1190	pF	$V_{DS} = 10 \text{ V}$
Output capacitance	$C_{oss}$	—	150	—	pF	$V_{GS} = 0$
Reverse transfer capacitance	$C_{rss}$	—	80	—	pF	$f = 1 \text{ MHz}$
Gate Resistance	$R_g$	—	1.55	3.1	$\Omega$	
Total gate charge	$Q_g$	—	7.1	—	nC	$V_{DD} = 10 \text{ V}$
Gate to source charge	$Q_{gs}$	—	2.3	—	nC	$V_{GS} = 4.5 \text{ V}$
Gate to drain charge	$Q_{gd}$	—	2.0	—	nC	$I_D = 15 \text{ A}$
Turn-on delay time	$t_{d(on)}$	—	2.8	—	ns	$V_{GS} = 10 \text{ V}, I_D = 7.5 \text{ A}$
Rise time	$t_r$	—	1.7	—	ns	$V_{DD} \approx 10 \text{ V}$
Turn-off delay time	$t_{d(off)}$	—	12.6	—	ns	$R_L = 1.3 \Omega$
Fall time	$t_f$	—	3.5	—	ns	$R_g = 4.7 \Omega$
Body–drain diode forward voltage	$V_{DF}$	—	0.84	1.09	V	$I_F = 15 \text{ A}, V_{GS} = 0$ <sup>Note4</sup>
Body–drain diode reverse recovery time	$t_{rr}$	—	8.1	—	ns	$I_F = 15 \text{ A}, V_{GS} = 0$ $di_F/dt = 500 \text{ A}/\mu\text{s}$

Notes: 4. Pulse test

## • MOS2

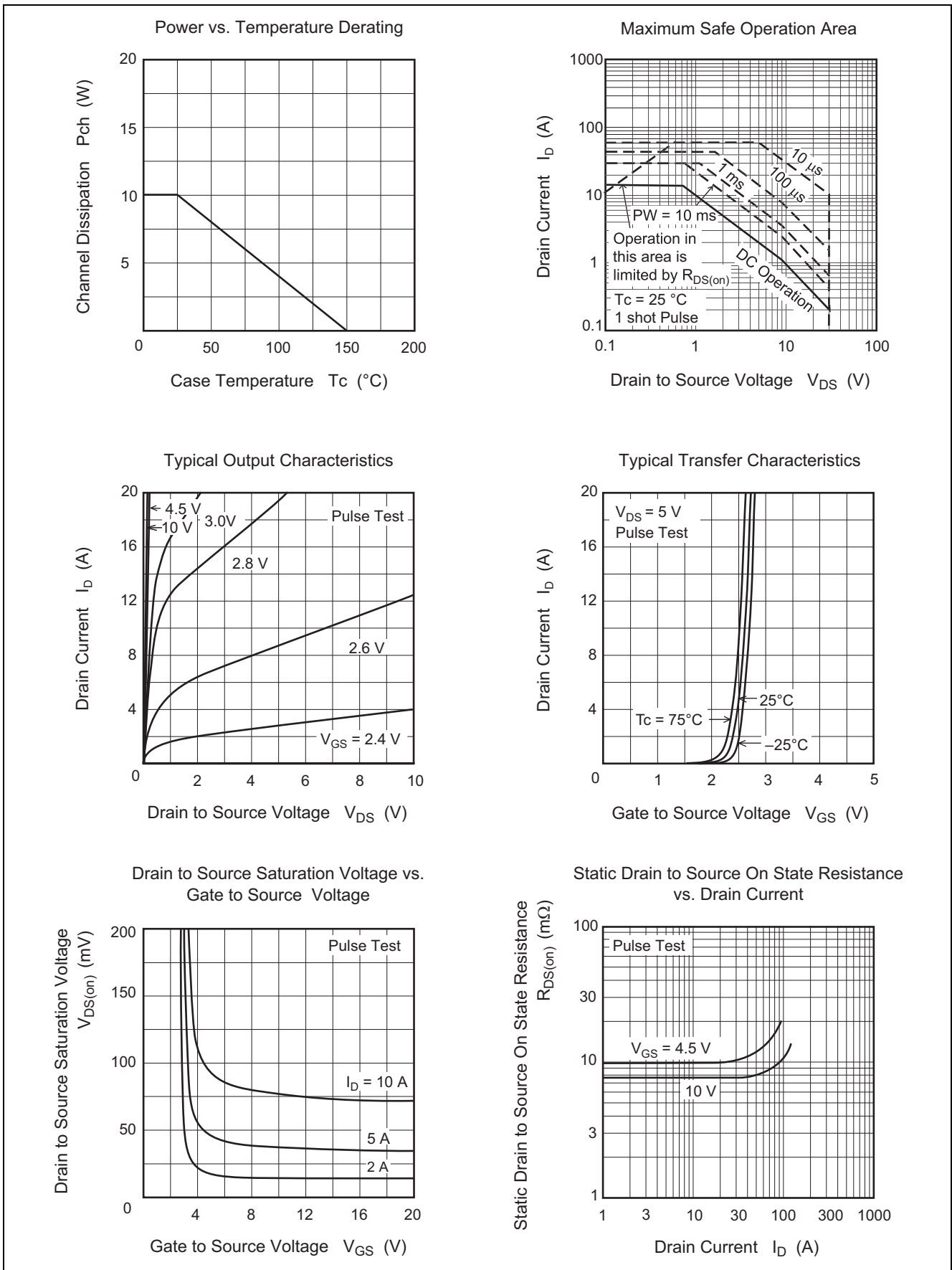
(Ta = 25°C)

Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	30	—	—	V	$I_D = 10 \text{ mA}, V_{GS} = 0$
Gate to source leak current	$I_{GSS}$	—	—	$\pm 0.5$	$\mu\text{A}$	$V_{GS} = \pm 20 \text{ V}, V_{DS} = 0$
Zero gate voltage drain current	$I_{DSS}$	—	—	1	mA	$V_{DS} = 24 \text{ V}, V_{GS} = 0$
Gate to source cutoff voltage	$V_{GS(off)}$	1.2	—	2.5	V	$V_{DS} = 10 \text{ V}, I_D = 1 \text{ mA}$
Static drain to source on state resistance	$R_{DS(on)}$	—	4.4	5.3	m $\Omega$	$I_D = 15 \text{ A}, V_{GS} = 10 \text{ V}$ <sup>Note4</sup>
	$R_{DS(on)}$	—	5.4	7.0	m $\Omega$	$I_D = 15 \text{ A}, V_{GS} = 4.5 \text{ V}$ <sup>Note4</sup>
Forward transfer admittance	$ y_{fs} $	—	65	—	S	$I_D = 15 \text{ A}, V_{DS} = 5 \text{ V}$ <sup>Note4</sup>
Input capacitance	$C_{iss}$	—	2110	2950	pF	$V_{DS} = 10 \text{ V}$
Output capacitance	$C_{oss}$	—	345	—	pF	$V_{GS} = 0$
Reverse transfer capacitance	$C_{rss}$	—	210	—	pF	$f = 1 \text{ MHz}$
Gate Resistance	$R_g$	—	1.5	3.0	$\Omega$	
Total gate charge	$Q_g$	—	16.5	—	nC	$V_{DD} = 10 \text{ V}$
Gate to source charge	$Q_{gs}$	—	5.3	—	nC	$V_{GS} = 4.5 \text{ V}$
Gate to drain charge	$Q_{gd}$	—	5.5	—	nC	$I_D = 30 \text{ A}$
Turn-on delay time	$t_{d(on)}$	—	4.7	—	ns	$V_{GS} = 10 \text{ V}, I_D = 15 \text{ A}$
Rise time	$t_r$	—	2.9	—	ns	$V_{DD} \approx 10 \text{ V}$
Turn-off delay time	$t_{d(off)}$	—	35.2	—	ns	$R_L = 0.7 \Omega$
Fall time	$t_f$	—	11.4	—	ns	$R_g = 4.7 \Omega$
Schottky Barrier diode forward voltage	$V_F$	—	0.46	—	V	$I_F = 2 \text{ A}, V_{GS} = 0$ <sup>Note4</sup>
Body-drain diode reverse recovery time	$t_{rr}$	—	6.6	—	ns	$I_F = 30 \text{ A}, V_{GS} = 0$ $di_F/dt = 500 \text{ A}/\mu\text{s}$

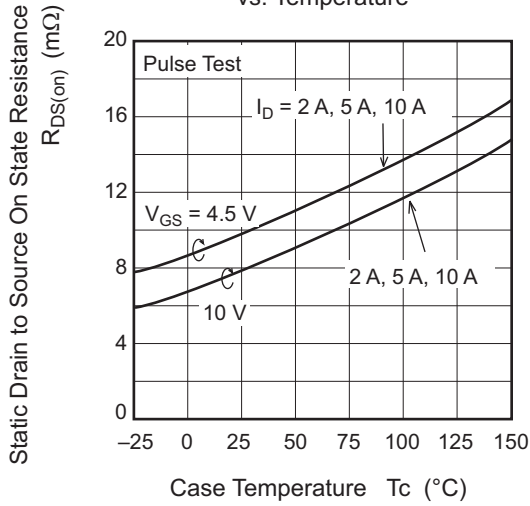
Notes: 4. Pulse

## Main Characteristics

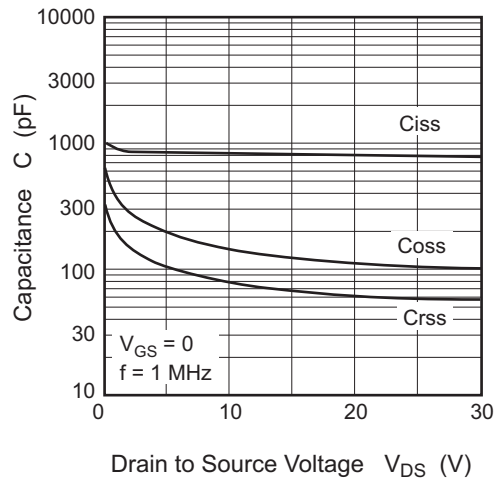
• MOS1



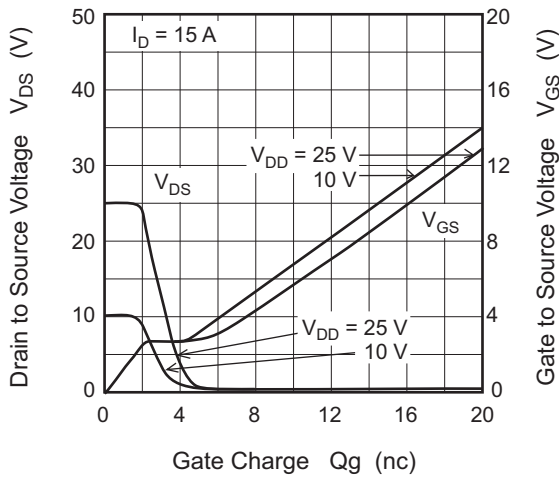
Static Drain to Source On State Resistance vs. Temperature



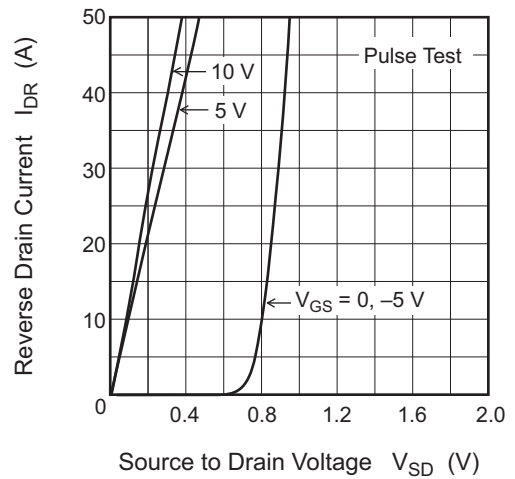
Typical Capacitance vs. Drain to Source Voltage



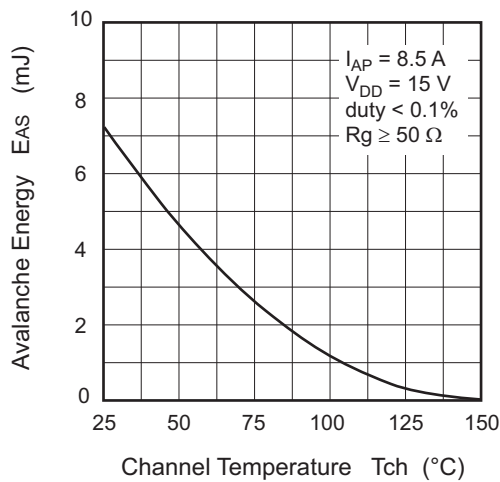
Dynamic Input Characteristics



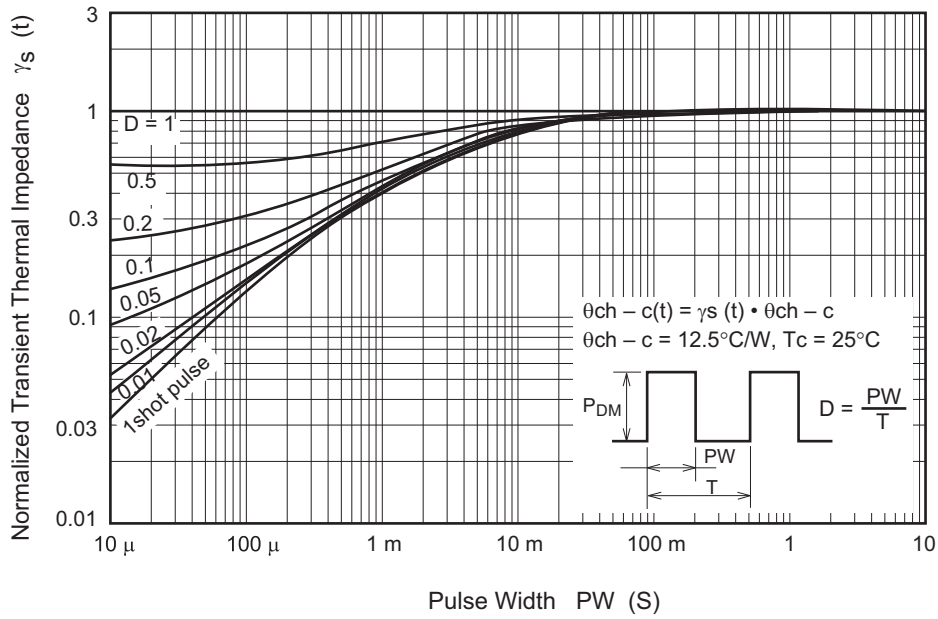
Reverse Drain Current vs. Source to Drain Voltage



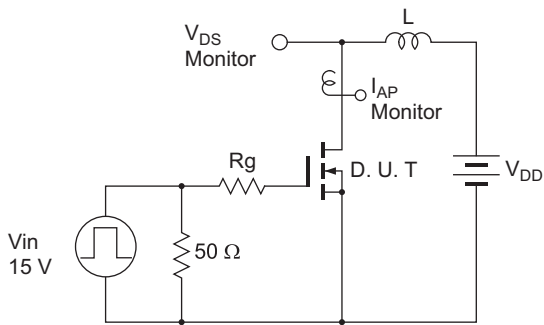
Maximum Avalanche Energy vs. Channel Temperature Derating



Normalized Transient Thermal Impedance vs. Pulse Width

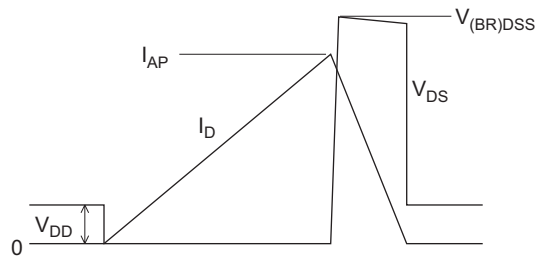


Avalanche Test Circuit

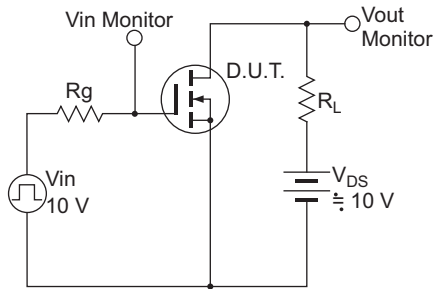


Avalanche Waveform

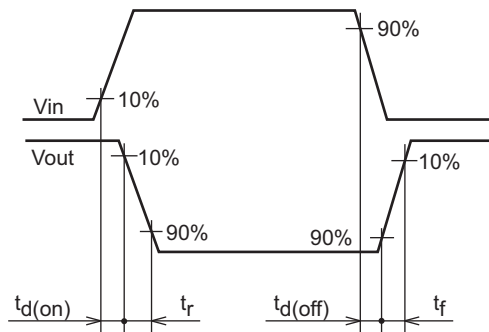
$$E_{AS} = \frac{1}{2} L \cdot I_{AP}^2 \cdot \frac{V_{DSS}}{V_{DSS} - V_{DD}}$$



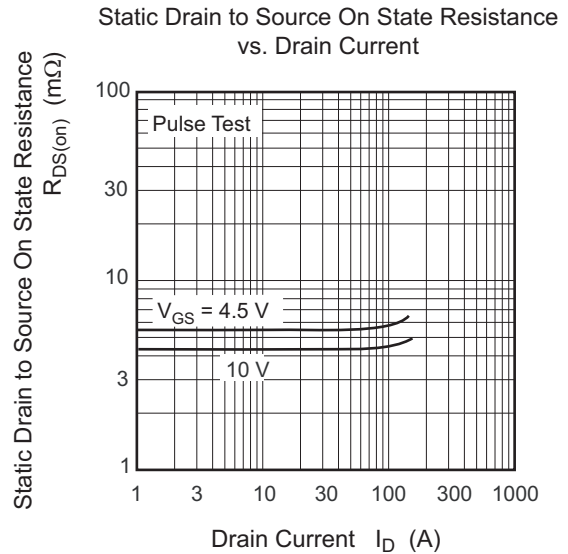
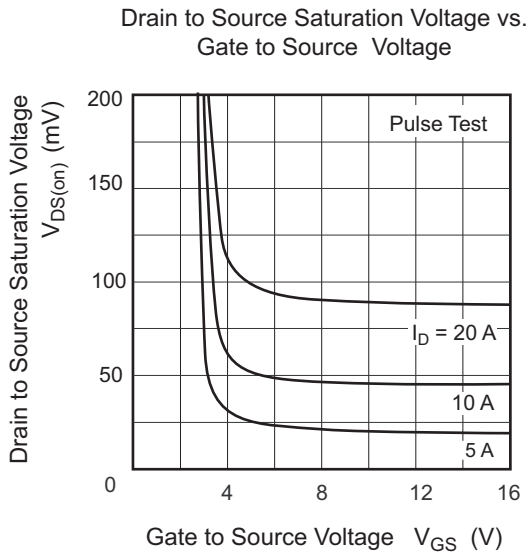
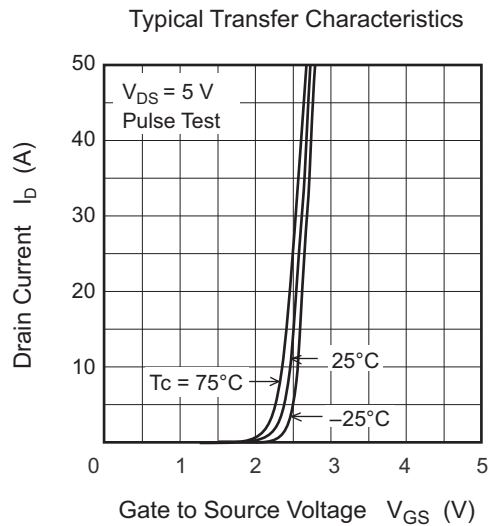
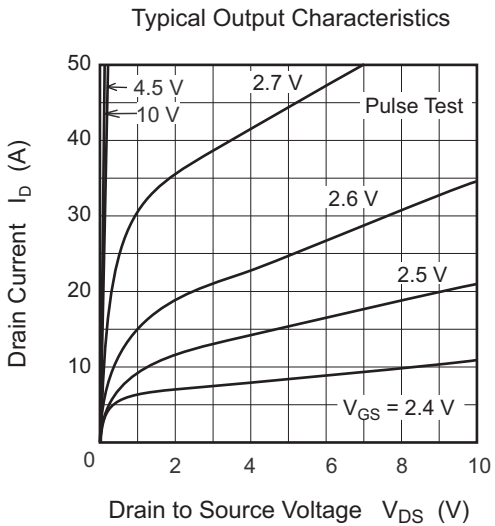
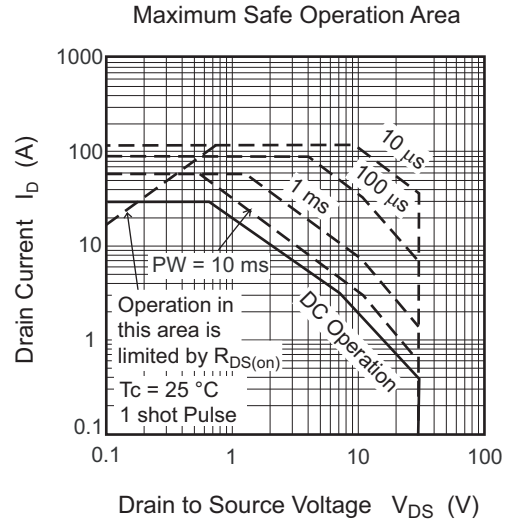
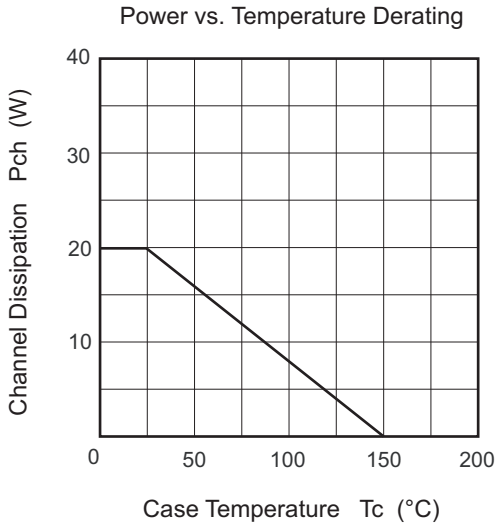
Switching Time Test Circuit

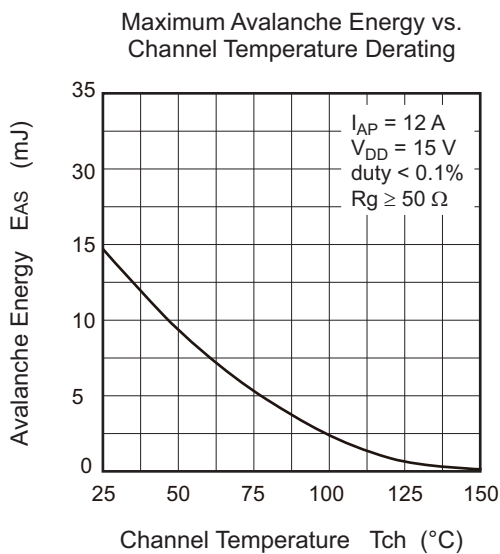
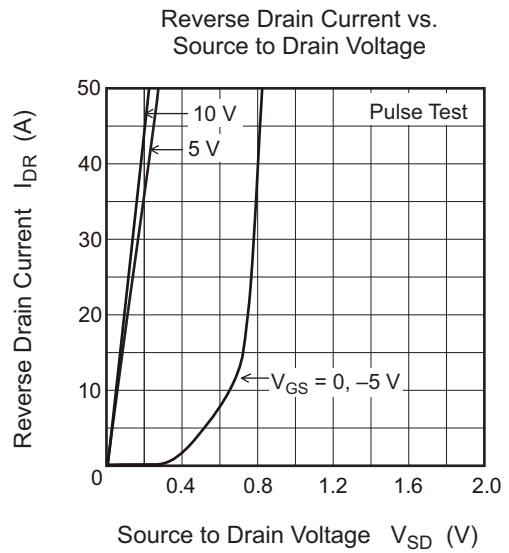
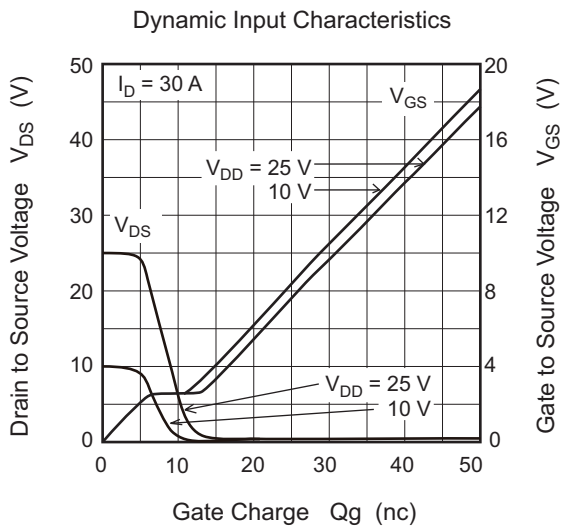
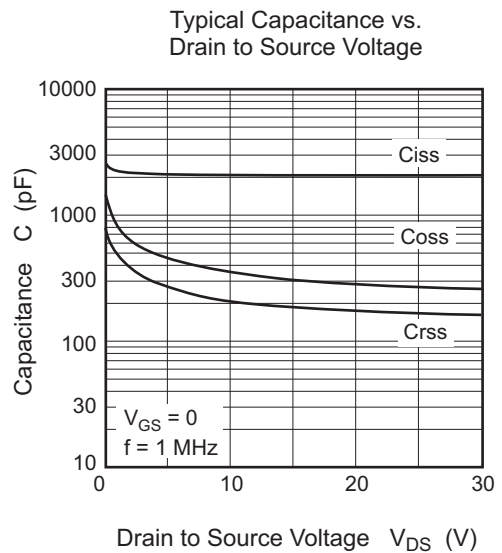
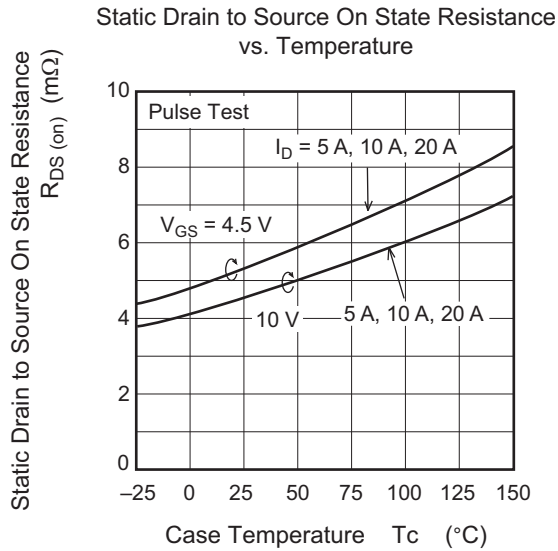


Switching Time Waveform



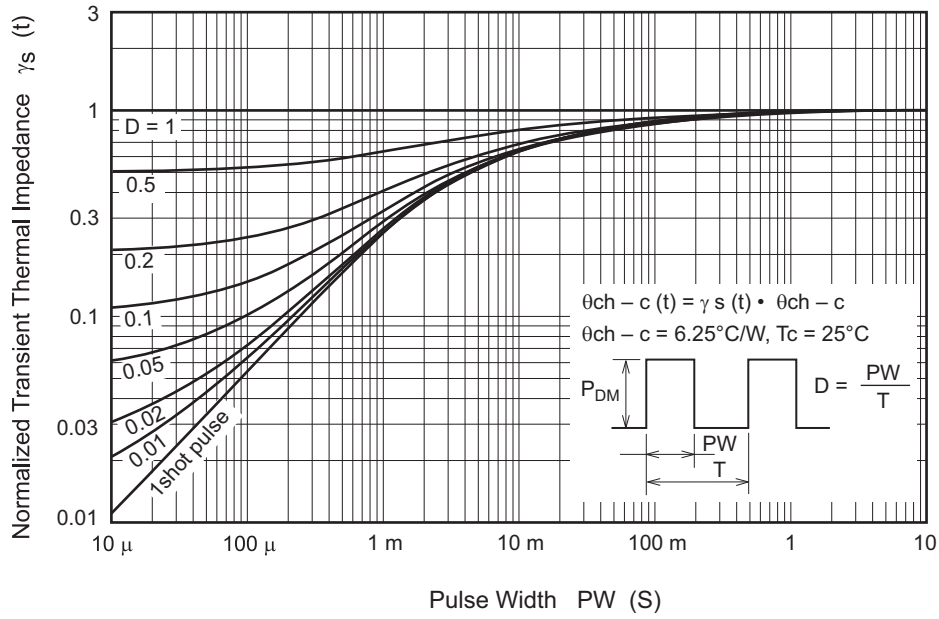
• MOS2 and Schottky Barrier Diode



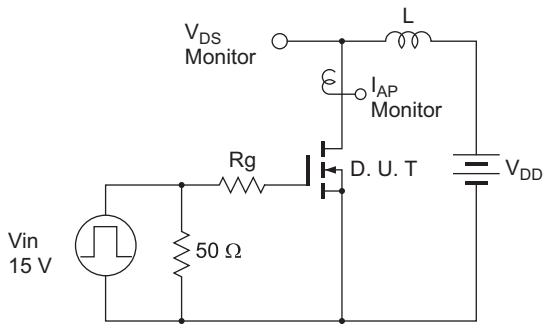




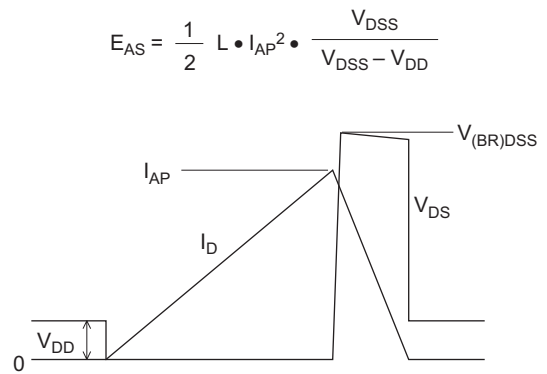
Normalized Transient Thermal Impedance vs. Pulse Width



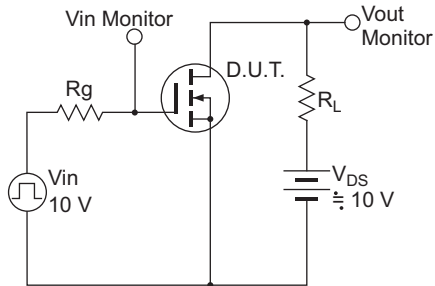
Avalanche Test Circuit



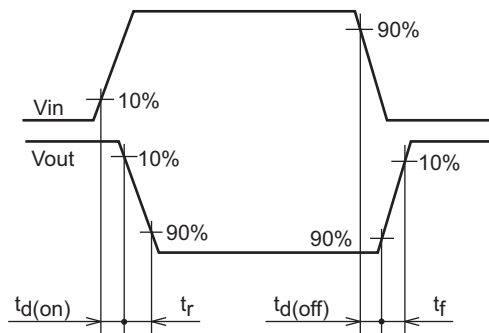
Avalanche Waveform



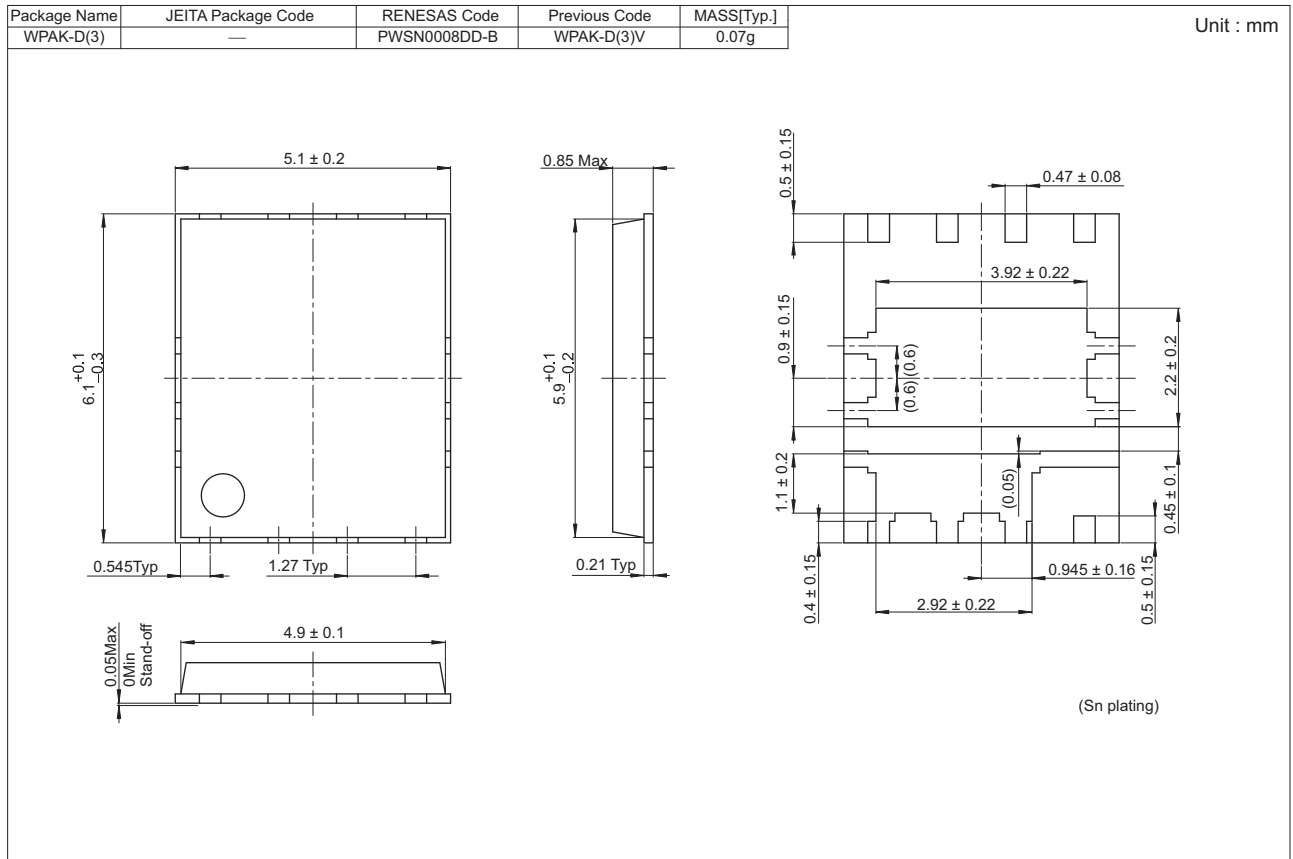
Switching Time Test Circuit



Switching Time Waveform



### Package Dimensions



### Ordering Information

Orderable Part Number	Quantity	Shipping Container
RJK03P7DPA-00-J5A	3000 pcs	Taping

Note: The symbol of 2nd "-" is occasionally presented as "#".

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